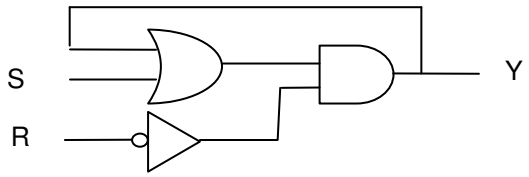
1S. Analyze the latch circuit shown below by obtaining timing diagram for the circuit; include propagation delays.

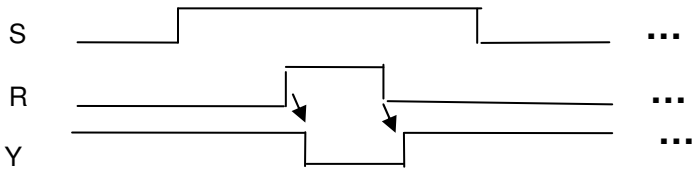


Solution:

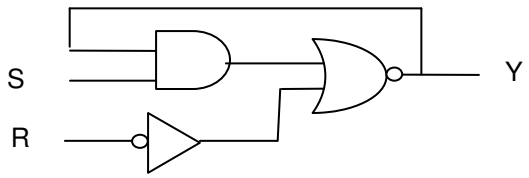
This circuit has two external input and one feedback input, therefore has total of 8 possible input conditions:

Input			Output
S	**R**	**Current Y**	**Next Y**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Corresponding Timing Diagram:



1U. Analyze the latch circuit shown below by obtaining timing diagram for the circuit; include propagation delays.

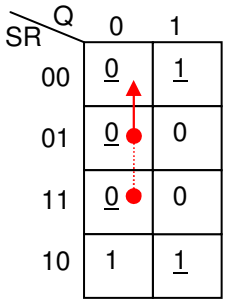


2S. Analyze the SR Flip-Flop circuit using K-map to determine if the input conditions SR=11 transition to SR=00 with initial state Q=0 can result in a critical race.

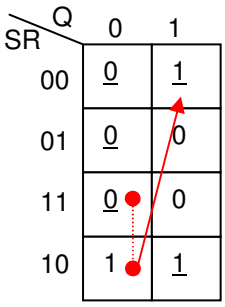
Solution:

S R Q = 110
SR are changed simultaneously to 00

- S may change first S R Q = 010 → Q+ = 0 Stable state
  next R changes, SRQ = 0 0 0 → Q+ = 0 Stable state



- R may change first S R Q = 100 → Q+ = 1 (unstable state).
  Next S changes, S R Q = 001 → Q+ = 1 (stable state).



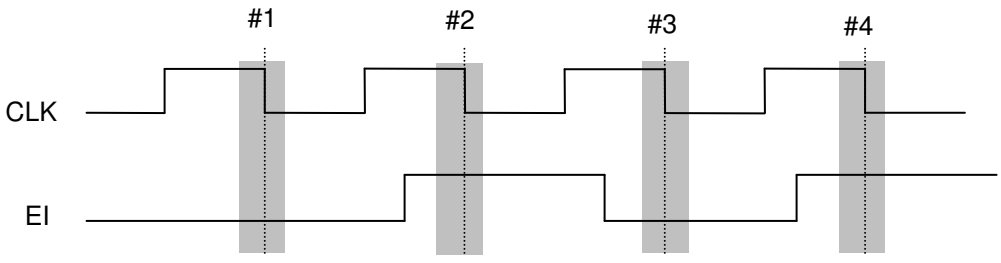
Note: Depending on if S changed first or R changed first, the final state will be different; therefore, we have a critical race.

2U. Analyze the SR Flip-Flop circuit using K-map to determine if the input conditions SR=00 transition to SR=11 with initial state Q=1 can result in a critical race.

Solution:

3S. Draw a clock signal CLK with four 1-to-0 timing events, a nonzero setup time, t_{su}, and a nonzero hold time, t_h. Also draw one excitation input signal EI that follows the sequence 0101 and meets the setup and hold time requirements. In the excitation input, the first bit in the sequence (0) occurs in time for the first clock timing event, the second bit in the sequence (1) occurs in time for the second clock timing event, and so forth.

Solution:

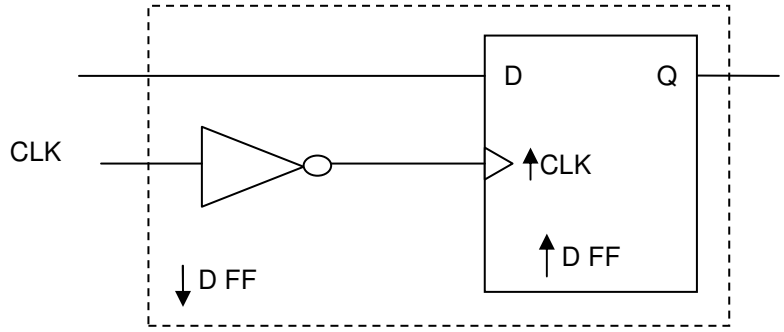


3U. Draw a clock signal CLK with five 0-to-1 timing events, a nonzero setup time, t_{su}, and a nonzero hold time, t_h. Also draw one excitation input signal EI that follows the sequence 10110 and meets the setup and hold time requirements. In the excitation input, the first bit in the sequence (1) occurs in time for the first clock timing event, the second bit in the sequence (0) occurs in time for the second clock timing event, and so forth.

Solution:

4S. Show how a positive-edge-triggered D flip-flop and an inverter can be used as a negative-edge D flip-flop.

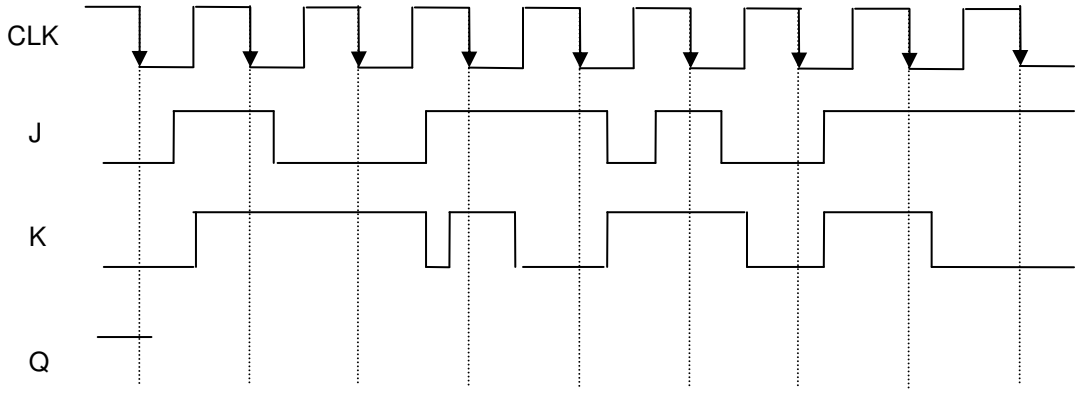
Solution:



4U. Show how a positive-edge-triggered D flip-flop and other logic gates can be used to design a positive-edge T flip-flop.

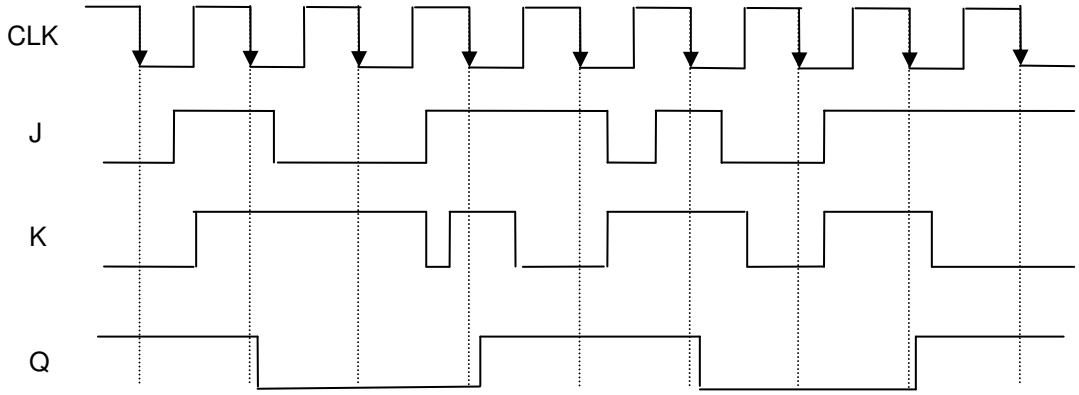
Solution:

5S. Complete the timing diagram shown below for a negative-edge-triggered J-K flip-flop. Assume that the J and K inputs always meet the setup and hold time requirements for the J-K flip-flop.
Hint: Use the JK flip-flop characteristic table.



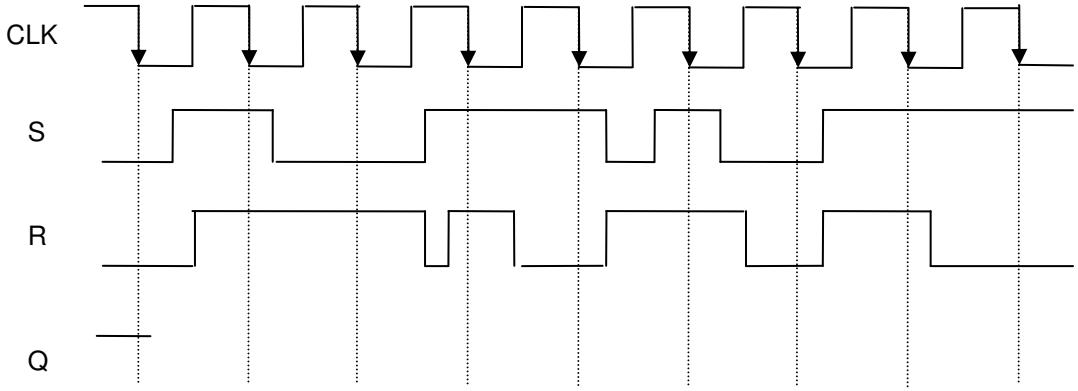
J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	Q'

Solution:



J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	Q'

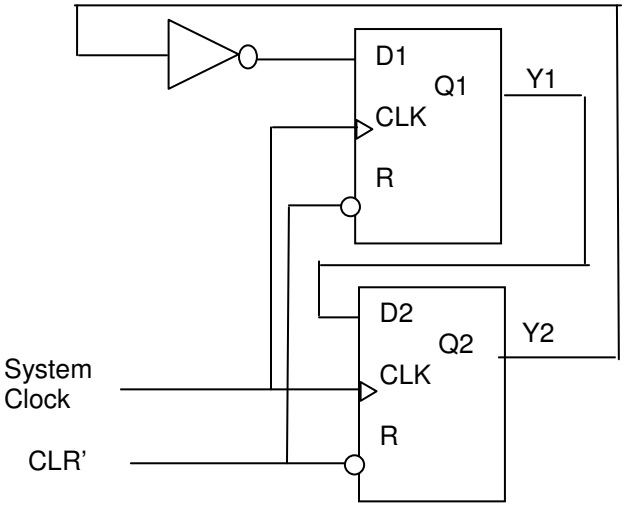
5U. Complete the timing diagram shown below for a negative-edge-triggered SR flip-flop. Assume that the S and R inputs always meet the setup and hold time requirements for the SR flip-flop.
Hint: Use the SR flip-flop characteristic table.



S	R	Q^+
0	0	Q
0	1	0
1	0	1
1	1	0

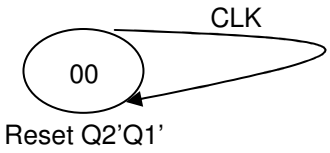
Solution:

6S. Obtain the state diagram for the circuit shown below.



Solution:

Case 1 State Diagram (when CLR' = 0):



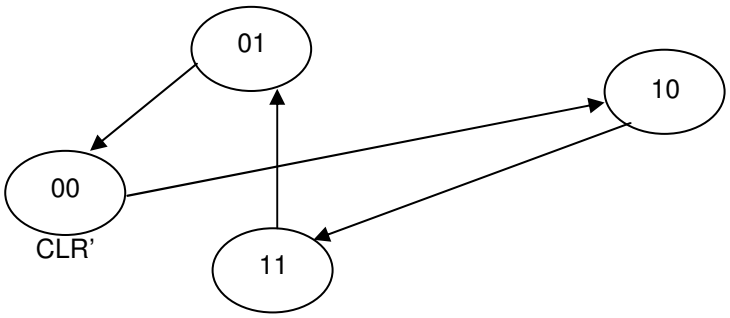
Case 2. State Diagram (when CLR' = 1):

$Q_1^+ = D_1 = Q_2'$

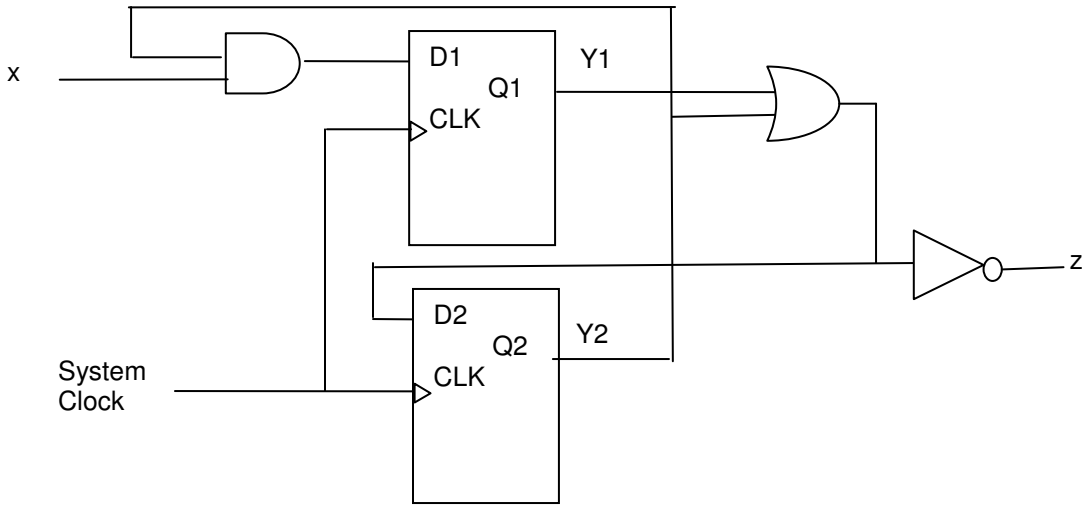
$Q_2^+ = D_2 = Q_1$

PS/NS Table

Q_1	Q_2	Q_1+	Q_2+
0	0	1	0
0	1	0	0
1	0	1	1
1	1	0	1



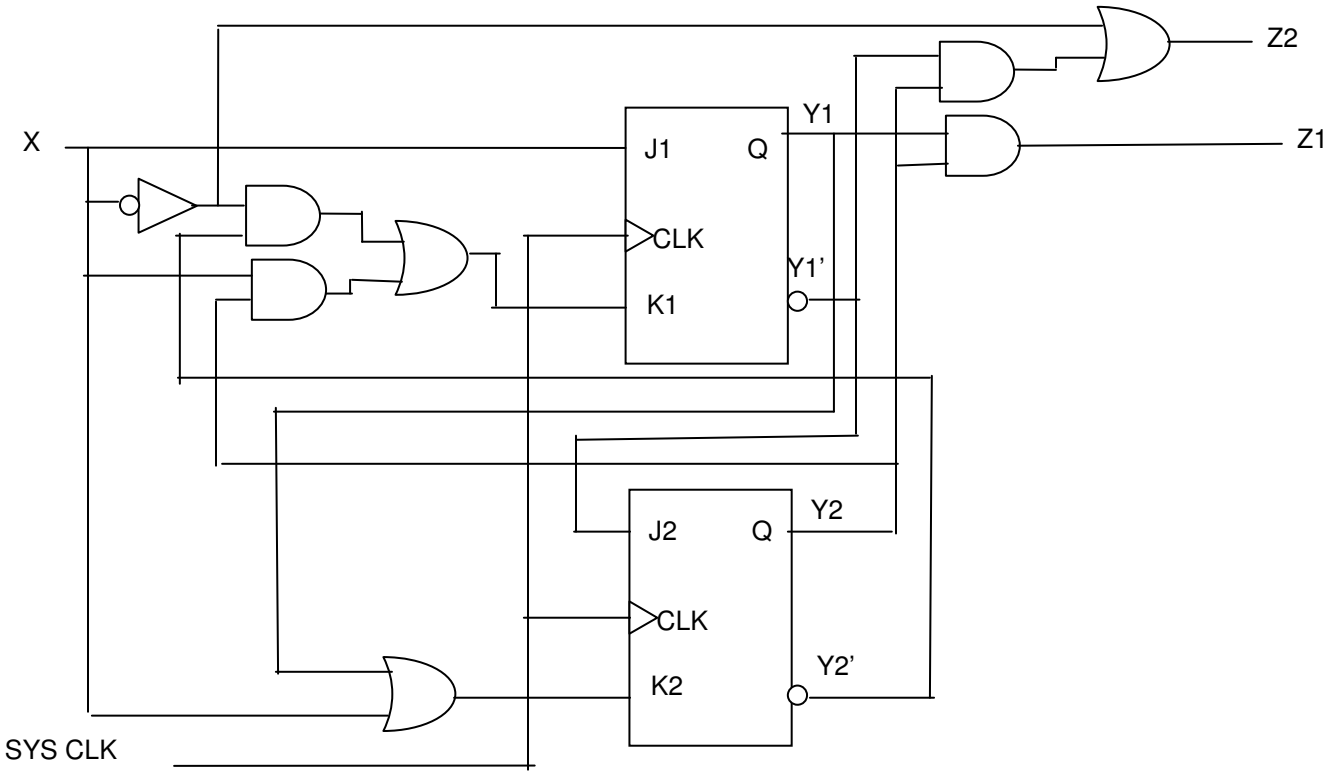
6U. Obtain the state diagram for the circuit shown below.



Solution:

7S. Analyze the state machine shown below to obtain the following items:

a) Excitation input and external output equations
b) PS/NS
c) State Diagram



Solution:

a)
Excitation Equations:
J1= X
K1 = X'.Y2' + X.Y2
J2 = Y1'
K2 = X + Y1

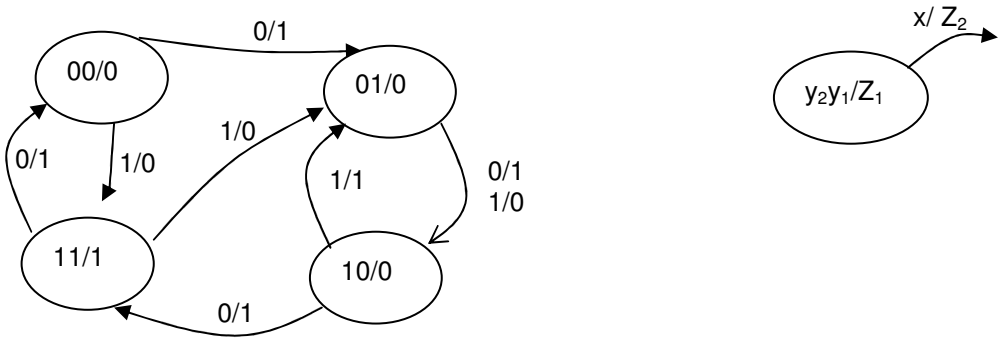
Apply the excitation equations into the JK ff Characteristic equation (Yi^+=Ji.Yi' + Ki'.Yi)
$Y1^+$ = X.Y1' + (X'.Y2' + X.Y2)'Y1
$Y2^+$ = Y1'.Y2' + (X + Y1)'.Y2

External Outputs
$Z_1 = Y_1.Y_2$
$Z_2 = Y_1'.Y_2 + X'$

b) PS/NS Table

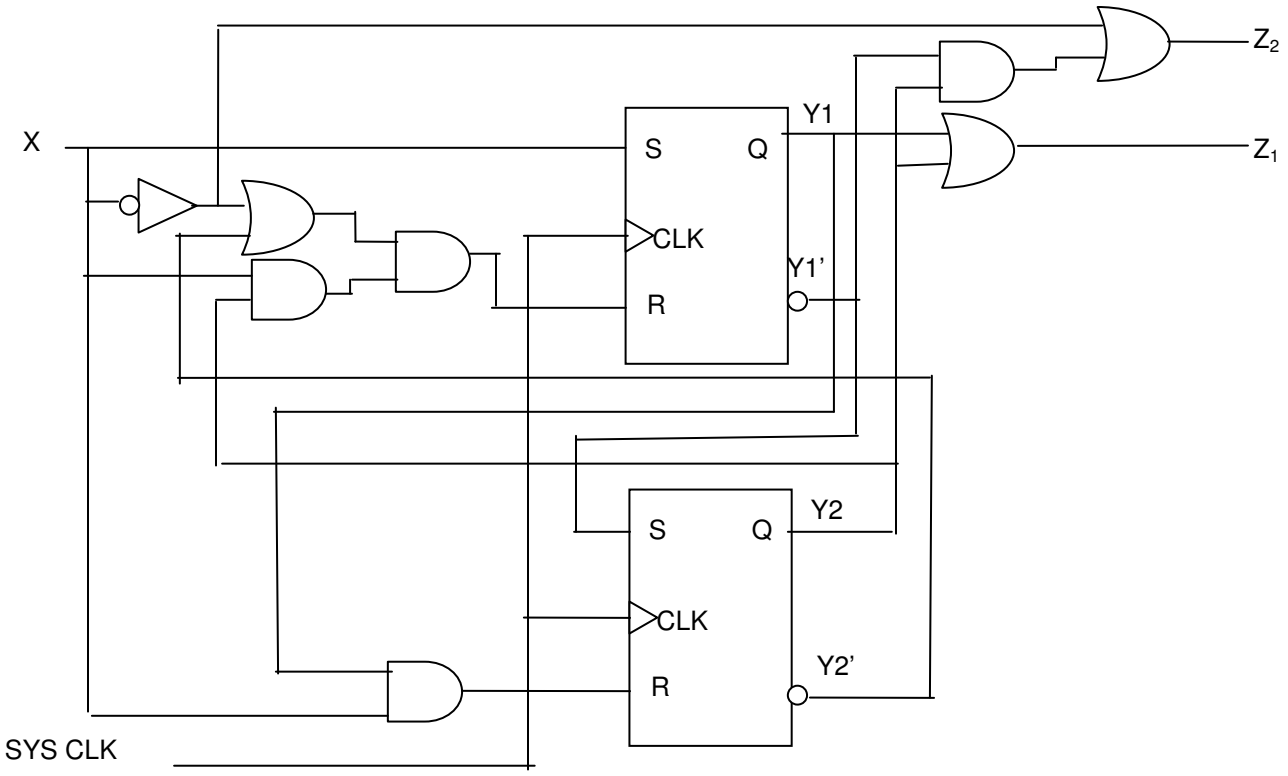
y_2	y_1	x	y_2^+	y_1^+	J_1	K_1	J_2	K_2	Z_1	Z_2
0	0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	1	0	1	1	0	0
0	1	0	0	0	0	1	0	1	0	1
0	1	1	1	0	1	0	0	1	0	0
1	0	0	1	1	0	0	1	0	0	1
1	0	1	0	1	1	1	1	1	0	1
1	1	0	0	0	0	0	0	1	1	1
1	1	1	0	1	1	1	0	1	1	0

c) State Diagram



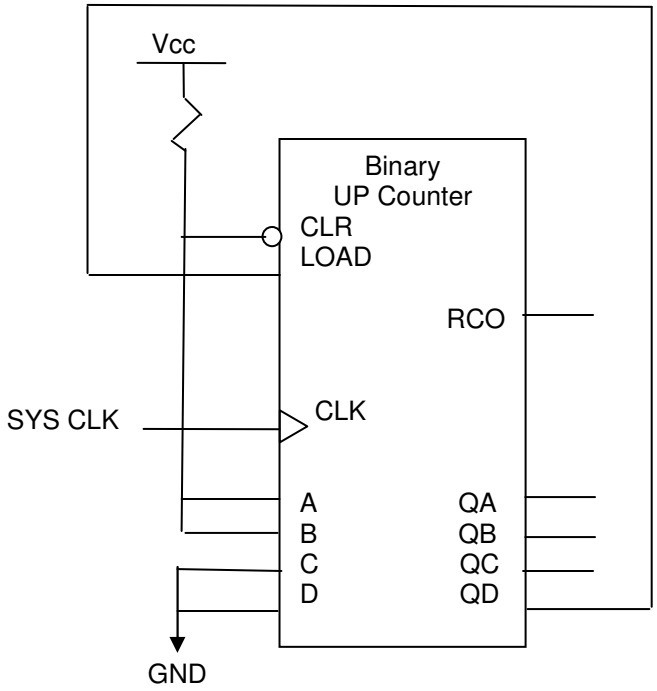
7U. Analyze the state machine shown below to obtain the following items:

a) Excitation input and external output equations
b) PS/NS
c) State Diagram



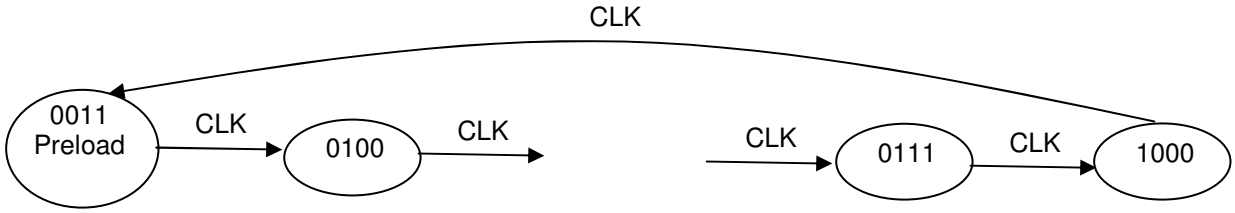
Solution:

8S. Obtain the state diagram for the circuit shown below. What is the mod of the counter? Is this counter useful? Change only the value being loaded at the inputs to obtain a mod 9 counter. What value must be loaded to do this?



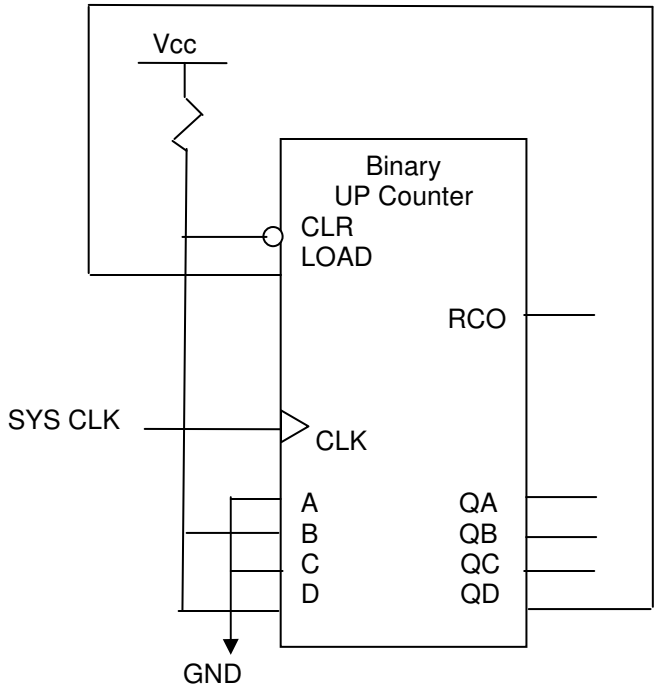
- CLR' and LOAD are synchronous inputs
- CLR' will set all output to 0
- LOAD allows values on A,B,C and D got to QA, QB, QC and QD.
- QD is MSB & QA is LSB

Solution:



Counter is a mod-6 counter (8 – 3 + 1).
It can be used to count from 3 to 8.
If A,B,C and D were grounded, then the counter would count from 0 to 8 (mod-9).

8U. Obtain the state diagram for the circuit shown below. What is the mod of the counter? Is this counter useful? Change only the value being loaded at the inputs to obtain a mod 9 counter. What value must be loaded to do this?



- CLR' and LOAD are synchronous inputs
- CLR'=0 will set all output to 0
- LOAD=1 allows values on A,B,C and D to pass through to QA, QB, QC and QD.
- QD is MSB & QA is LSB

Solution:

9S. What is the frequency of the fastest clock for a circuit using D flip flops with t_{hold} =5 nsec. and t_{setup} = 10 nsec. Assuming there are no other limitations.

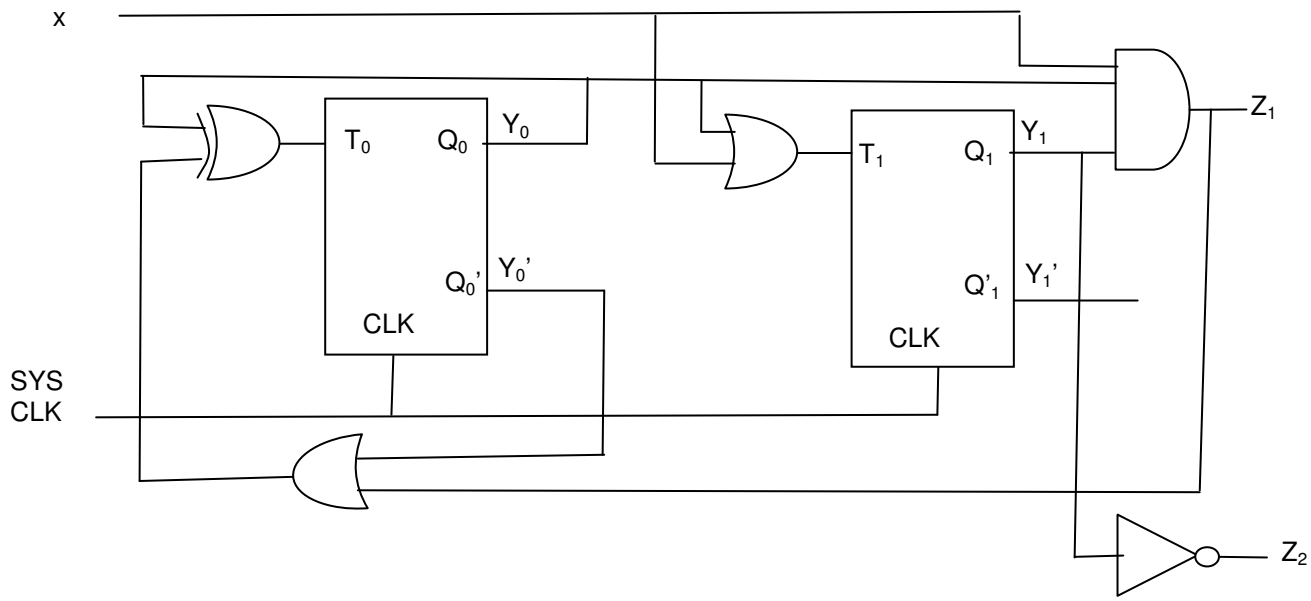
Solution:

Tclk > 15 nsec. → fclk < 10^9/15 or 66.67 Mhz

9U. What is the frequency of the fastest clock for a circuit using D flip flops with t_{hold} =50 psec. and t_{setup} = 150 psec. Assuming there are no other limitations.

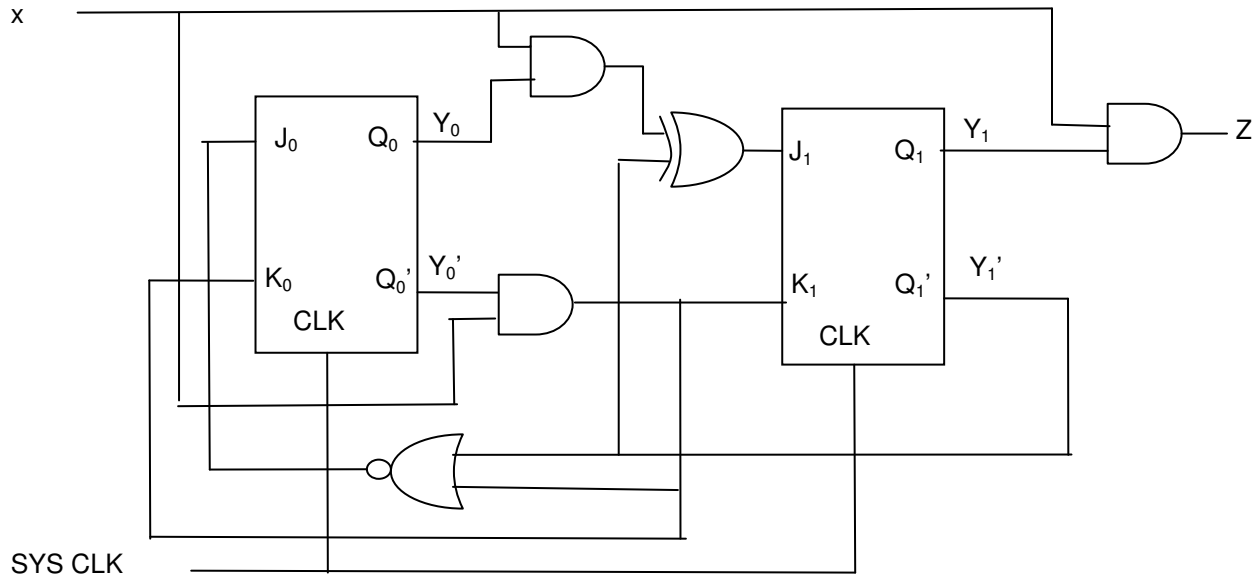
Solution:

10U. Analyze the following logic circuit:



Solution:

11U. Analyze the following logic circuit:



Solution: