Digital Logic Design LAB #7 - Verilog

Objective
The objective of this lab is to introduce students to Verilog Hardware Description Language (Verilog) development environment in order to analyze and synthesize combinational and sequential logic.

Related Principles & Resources
- Combinational and sequential logic circuit design
- Verilog Reference Guide in the Active-HDL application (Help)
- Data entry and simulation Tutorial in the Active-HDL application (Help>On-line Documentation>Verilog Entry Tutorial)

Equipment & Preparation
- Windows-based PC
- All lab computers have Active HDL installed. Students can also download a free version of Aldec Active-HDL Student Edition from www.Aldec.com for personal use only. If you download from Aldec.com and follow the application instruction for installation, it is important to do the following before your first design:
  *** select "Tools→Preferences→Access to Design Objects". Uncheck "Limit read access to design top-level signals only" and check all three check boxes under "Enable Access". Then press "Apply" button. Now you are ready to enter and simulate your design. ***
- USB hard disk or other removable drives
- Review Lecture and text material on Verilog

Experiment #1
Complete the example presented in Active-HDL "Verilog Entry tutorial" through "Simulation" section. Document the system that is being designed in the tutorial. The resulting system documentation should include a block diagram and explanation of input and output ports.
Hint: Use" help>online documentation" menu and search for "Verilog Entry Tutorial".

Experiment #2
Design and create simulation waveform for an Exclusive NOR using Verilog.

Experiment #3
Design and create a simulation waveform for a 3 out of 12 event detector using Verilog. This system will assert output to 1 when exactly 3 out of the last 12 serial events (value of input during a 12 past rising edge of clock) have been 1s.

Report Requirements
All reports must be computer printed (Formulas and Diagrams may be hand drawn) and at minimum include:

For each Experiment
a) Clear problem statement; specify items given and to be found.
b) Identify the theory or process used.
c) Documents resulting system diagram, schematics, tables, timing diagram, schematic and other relevant results.

For the report as a whole
a) Cover sheet with your name, course, lab, date of completion and team members' names.
b) Lessons Learned from the experiments.
c) A new experiment and expected results which provide additional opportunity to practice the concepts in this lab.