Digital Logic Design Lab #5

Objectives

1) Application of encoder/decoders, counters in a synchronous logic circuits
2) Proficiency in requirement analysis, logic design, implementation and testing processes.

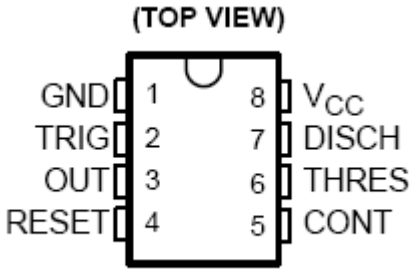
Materials

1) Textbook: Digital Logic Design by Khormaee.
2) Course Website: www.EngrCS.com
3) Instruments: Power Supply, Function Generator and Oscilloscope
4) Supplies:
   a) Proto Board (1 unit)
   b) Jumper Wires (as needed)
   c) Assorted LED Colors (8 units)
   d) 1 KΩ resistor (8 units)
   e) 1 MΩ resistor (2 units)
   f) 0.01 uF capacitor (1 unit)
   g) 1 uF capacitor (1 unit)
   h) NE 555P, 74LS93, 74LS138 (1 unit)
   i) 74LS00 through 74LS32 (as needed)

Notice: Ground and Vcc pin #s varies among the ICs so double check your schematic and design before powering your Design.

Experiment #1. NE 555 P Astable Operation (Clock generator application)

Implement the following design to generate a clock signal where t_L is the low and t_H is the high part of period. This clock generator will be used later in this so it should be set up at one end of the proto board.



Device #	Pin#	Value
U1	1	GND
U1	3	Out
U1	8	Vcc
U1	5	Open

$t_H = 0.693 (R_A + R_B) C$

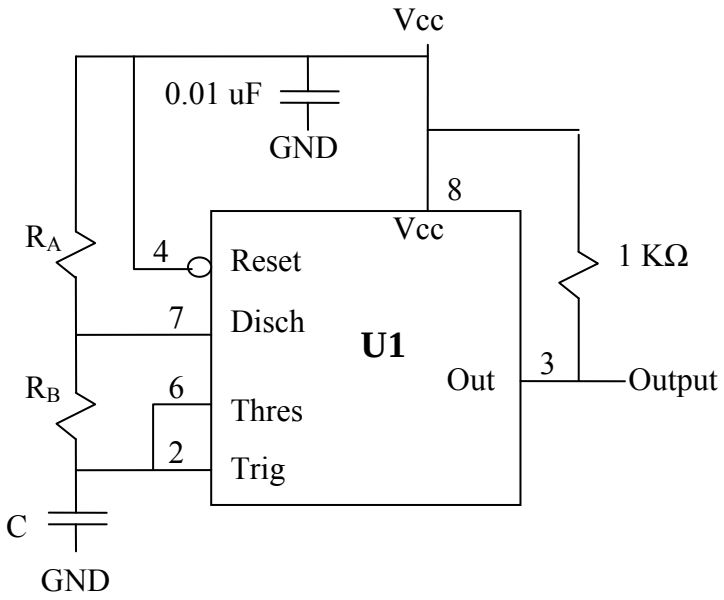
$t_L = 0.693 (R_B) C$

where

R_A = 1 MΩ

R_B = 1 MΩ

C = 1 UF



Calculate and draw the clock signal based on the formulas provided. Compare the clock signal waveform observed on the output pin of NE 555 with the calculated waveform. Explain reasons for differences between the two waveforms.

Experiment #2. Sequencing Light System

Use the 74LS138 (3 to 8 Decoder), 74LS93 (4-bit binary counter) and the clock generator from experiment #1 to implement an 8-LED sequencing light. Each light should turn on for a period of approximately 1-2 seconds. However any given light should not be off more than 16 seconds. LEDs must turn on in sequence as it is layout on the Proto Board. Your deliverables for this lad should include:

a) A system diagram with clearly identified independent variables (input) and dependent variables (output).
b) A detailed schematic, timing diagram and test plan for the Sequencing Light System.
c) Implement and test your design from previous step.
d) Demonstrate your final circuit for the instructor.

Experiment #3. Design of "2-bit binary adder with carry" using a PLD

Redo your design from Lab #4 "2-bit binary adder with carry" using your choice of PLD. Your deliverables should include:

1) Explanation of your PLD-type selection in-term of cost (requires pricing research) and ease-of-implementation.
2) Your output functions (POS or SOP).
3) Design schematics and PLD fuse map(s).

Report Requirements

All reports must be computer printed (Formulas and Diagrams may be hand drawn) and at minimum include:

For each Experiment

a) Clear problem statement; specify items given and to be found.
b) Identify the theory or process used.
c) Documents resulting system diagram, schematics, tables, timing diagram, schematic and other relevant results.

For the report as a whole

a) Cover sheet with your name, lab, date of completion and team members' names.
b) Lessons Learned from the experiments.
c) A new experiment and expected results which provide additional opportunity to practice the concepts in this lab.